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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.	
10/612,793	07/02/2003	Arup Bhattacharyya	1303.111US1	5437	
7590 08/27/2004			EXAMINER		
Schwegman, Lundberg, Woessner & Kluth, P.A.			ERDEM	ERDEM, FAZLI	
Attn: Marvin L. Beekman P.O. Box 2938		ART UNIT	PAPER NUMBER		
Minneapolis, MN 55402			2826		

DATE MAILED: 08/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<del></del>	Application No.	Applicant(s)	
	10/612,793	BHATTACHARYYA, ARUP	
Office Action Summary	Examiner	Art Unit	1
	Fazli Erdem	2826	And I
The MAILING DATE of this communication app Period for Reply	ears on the cover sheet with the	correspondence a	ddress
A SHORTENED STATUTORY PERIOD FOR REPLY THE MAILING DATE OF THIS COMMUNICATION.  - Extensions of time may be available under the provisions of 37 CFR 1.13 after SIX (6) MONTHS from the mailing date of this communication.  - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period was - Failure to reply within the set or extended period for reply will, by statute, Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b).	36(a). In no event, however, may a reply be within the statutory minimum of thirty (30) dwill apply and will expire SIX (6) MONTHS from a cause the application to become ABANDON	timely filed lays will be considered time om the mailing date of this o NED (35 U.S.C. § 133).	•
Status			
Responsive to communication(s) filed on 22 M     This action is <b>FINAL</b> . 2b) ☑ This     Since this application is in condition for allowar closed in accordance with the practice under E	action is non-final. nce except for formal matters, p		e merits is
Disposition of Claims			
<ul> <li>4)  Claim(s) 1-100 is/are pending in the application 4a) Of the above claim(s) 80-100 is/are withdra</li> <li>5)  Claim(s) 6-53, 72-79 is/are allowed.</li> <li>6)  Claim(s) 1-5 and 54-71 is/are rejected.</li> <li>7)  Claim(s) is/are objected to.</li> <li>8)  Claim(s) are subject to restriction and/or</li> </ul>	wn from consideration.		
Application Papers			
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acce Applicant may not request that any objection to the Replacement drawing sheet(s) including the correction 11) The oath or declaration is objected to by the Examine	epted or b) objected to by the drawing(s) be held in abeyance. So ion is required if the drawing(s) is d	See 37 CFR 1.85(a). Objected to. See 37 C	` '
Priority under 35 U.S.C. § 119			
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of:  1. Certified copies of the priority documents 2. Certified copies of the priority documents 3. Copies of the certified copies of the priority application from the International Bureau * See the attached detailed Office action for a list of the priority documents.	s have been received. s have been received in Applicative documents have been receing (PCT Rule 17.2(a)).	ation No ved in this National	l Stage
Attachment(s)  1) Notice of References Cited (PTO-892)  2) Notice of Draftsperson's Patent Drawing Review (PTO-948)  3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  Paper No(s)/Mail Date 03/01/2004.	4) Interview Summa Paper No(s)/Mail 5) Notice of Information 6) Other:	Date	O-152)

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#### **DETAILED ACTION**

#### Allowable Subject Matter

1. Claims 6-53 and 72-79 allowed.

2. The following is a statement of reasons for the indication of allowable subject matter:

Regarding Claim 6, prior art failed to establish a memory cell having first diffusion region connected to bit line, a second diffusion region which store the memory state of the memory cell, a negative differential resistance diode with an intrinsic region between the anode and cathode to assist with stabilizing the memory stat of the memory cell, connected between the second diffusion region and the reference potential line.

Regarding Claims 7-53, prior art failed to establish a p-channel or n-channel access transistor with a first and second p or n-type diffusion region where the second p or n-type diffusion region store the memory state of the memory cell and a negative differential resistance n/i/p or p/i/n diode having n or p-type anode and cathode with an intrinsic region between the anode and cathode to assist with stabilizing the memory state of the memory cell.

Regarding Claims 72-79, prior art failed to establish a memory device with memory array, word lines, bit lines with access transistor with first and second diffusion regions, a negative differential resistance diode with an intrinsic region between the anode and the cathode where the memory cell is used to store charge in the second diffusion region.

### Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-5 and 54-71 rejected under 35 U.S.C. 103(a) as being unpatentable over Han (6,611,452) in view of Babcock et al. (6,660,616).

Regarding Claims 1-5 and 54-71, Han discloses reference cells fro TCCT based memory cells where a reference cell produces a voltage rise on a bit line that is proportional rise on a another bit line produced by a TCCT based memory cell in an "on" state. The reference cell includes an NDR device, a gate line device disposed adjacent to the NDR device, a first resistive element coupled between the NDR device and the bit line, and a second resistive element coupled between a sink and the bit line. Han fails to disclose the required intrinsic region requirement. However, Babcock et al. disclose a P-I-N transit time silicon-on-insulator device where in columns 3 and 5, the required intrinsic region configuration is disclosed.

It would have been obvious to one of having ordinary skill in the art at the time the invention was made to include the required intrinsic region configuration in Han as taught by Babcock et al. in order to have a memory cell with higher performance.

## Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fazli Erdem whose telephone number is (703) 305-3868. The examiner can normally be reached on M - F 8:00 - 5:00.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

FE May 30, 2004

SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800